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Design and fabrication of quantum dot single electron transistor structure using e-beam nanolithography

U. Hashim*, S. Madnasri, Z. A. Z. Jamal

Institute of Nano Electronic Engineering, Universiti Malaysia Perlis, 01000, Kangar, Perlis, Malaysia.

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Abstract

Quantum dot single electron transistor (QD SET) is fabricated using e-beam nanolithography (EBL) and is continued with the combination process of pattern dependent oxidation (PADOX) and high density plasma etching. EBL was used to pattern the whole masks of SET fabrication which consist of mask for doped area separator and the rest are for the formation of: source-quantum dot-drain, poly-Si gate, point contact and metal pad respectively. All of these masks were designed using offline GDSII Editor Software and later been exposed by EBL integrated using the scanning electron microscopy (SEM). In this paper, the whole designs of SET masks which are successively patterned are demonstrated and their nanostructures characterizations using SEM and atomic force microscopy (AFM) are reported. We found that the shape and dimension biases of schematics and SEM images of masks were caused by proximity effect. Therefore, while designing the SET masks, proximity effect, used resist and EBL equipment resolutions were considered.

Keywords: E-beam lithography; Mask design; PADOX; Proximity effect; Quantum dot; Single electron transistor.
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1. Introduction

There are three common types of SETs namely nano-wire, carbon nano-tube (CNT) and QD SET. Theoretically, a SET consists of three capacitors, a conventional gate capacitor and two tunneling capacitors forming source and drain [1,18]. Two different methodologies have been proposed in the literature for the fabrication of silicon quantum dots: (i) a bottom up and (ii) top-down approach. The charging islands in SETs may be defined either by using high-resolution lithography, or 'naturally' by using the material nano-morphology [4]. EBL is the most commonly used technique in this field, and many researchers have been investigated on how to use it to design nanopatterns, such as Fulton and Dolan made SETs using an offset mask technique [19]. By using EBL to define the quantum dot instead of stress dependent oxidation rate, the size and shape of the dot can better controlled [7]. PADOX is one of reliable techniques to realize a well-defined silicon dot [6]. EBL is currently the production technique of masks used for other kinds of lithography. Its resolution will

*) For Correspondence, E-mail: uda@unimap.edu.my.

mean that it is always the choice for direct-write one-off production [14]. The amount of masks used in SET fabrication process depends significantly on each route of its process where as the amount of masks decrease, SET fabrication process will be simpler. Several attempts have therefore been made to develop a technique where different layers or function parts of the SET device are prepared in separate lithography steps [22]. In general, researchers have used some masks in their SETs fabrication such as three masks are each used for point contact pad [17,18], poly-Si gate [10,2] and metal pad formation [16] and the others are each used for ion implantation [18,16] and plasma oxide mask for Si etching [15,11] or defining Si structure [10]. There are additional masks in SET fabrication namely aluminium sacrificial [5,21] or suspended mask [12]. The gate poly-Si was lithographically patterned and etched to cover the Si quantum dot [10,20]. Constrictions as tunnel barriers can be fabricated by etch mask which is defined using EBL [3, 23]. Layer by layer alignment of SET fabrication was accurately adjusted using registration marks formed in the corners of the exposed area [15]. Markers are carefully engineered to survive the subsequent processing [16]. In this paper, we will describe the whole masks used in our SET fabrication.

2. Experimental procedures

Square substrates 15 mm x 15 mm in size were prepared from silicon wafer as the starting material. The specification of the used silicon wafer is crystal orientation of <100>, type/dopant of P/B, diameter of 525 +/- μm, and resistivity of 1 ~ 10 ohm-cm. Substrates made in square form are easier to pose in adjusting the stage position when focusing SEM image, by this, means we will observe design pattern on the developed resist. Wafer silicon was cut by means in parallel to the shortest wafer diameter. This is done to prevent the wafer from broken.

First, wafer is cleaned to remove either organic or inorganic contaminants using standard cleaning 1 in which the process series are as the following: dip in RCA-1 solution at temperature 75°C for 10 minutes, rinse in de-ionized (DI) water, dip in buffer oxide etch (BOE) for 10-15 minutes, rinse in DI-water, dip in RCA-2 solution at temperature 80°C for 10-15 minutes, rinse in DI-water and then spin drying. RCA-1 and RCA-2 solutions were heated up to 75°C and 80°C using corning hotplate.

The dried substrates were heated up to 200°C for 30 minutes using conduction hotplate JB-TEK Honeywall. Then those silicon substrates were cooled until room temperature. Negative tone ma-N 2403 resists were spun on the silicon substrates using spinner model WS-400B-GNPP/UTE/10K. Spin coater was set up on the ramp up 500 rpm for 6 seconds, spin speed 3000 rpm for 30 seconds and ramp down 0 rpm for 5 seconds. The deposited resist was pre-baked on the hot plate JB-TEK Honeywall at temperature 90 °C for 120 seconds to improve the film adhesion on the substrates. Thereafter, the uniform resist was cooled until room temperature, and then the resist is ready to be exposed using EBL. Meanwhile, mask 4 is spun with PMMA positive resist on the ramp up 500 rpm for 6 seconds, spin speed 4000 rpm for 30 seconds and ramp down 0 rpm for 5 seconds.

Masks were designed using offline GDSII Editor Software by considering proximity effects, optimum resolution of resist and e-beam equipment. In this research, we have fabricated five masks namely one mask for doping insulating and the others were each used for formation: source-QD-drain, poly Si gate, point contact and Al metal pad formation. The reason for the size difference is considered to be the effects of the resolution of the lithography. The optimum resolution of ma-N 2403 negative resist is 50 nm and minimum area step size of version 4.0 Raith software of EBL is 40 nm. Single quantum dot was designed in the range of this equipment resolution. Usually, resist pattern widths of SEM micrograph im-

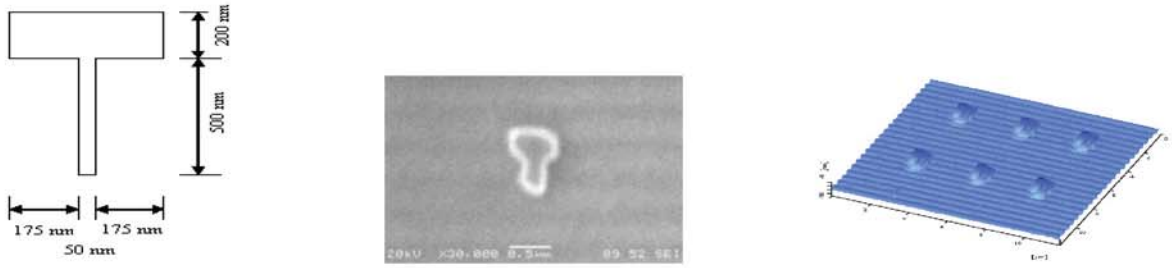
ages are wider of about 80 nm than that of GDSII design. Mask 4 was specifically spun of 495 PMMA (polymethylmetacrylate) A4 resist 4% in anisole and the others were spun of ma-N 2403 negative resist.

Samples have been already exposed using EBL in exposure parameters as the following: accelerating voltage of 20 kV, spot size of 45, field size of 200 μm, microscope magnification of 450X and e-beam dose in the range of 180-235 $\mu As/cm^2$. After e-beam exposure, SEM vacuum chamber vented to take out sample. Subsequently, samples were developed in ma-D 532 solution for 35-55 seconds and dipped in DI-water for 5-10 minutes to stop image development. Mask 4 was developed in a methyl-isobutyl-ketone (MIBK, PMMA solvent) mixed with three parts of isopropyl alcohol (IPA, non solvent) to obtain higher contrast [13] for 30 seconds and then dipped in IPA for 15-30 seconds.

The developed nanostructures were characterized by using scanning electron microscopy (JEOL SEM 6460LA) and atomic force microscopy (AFM SPI Probe Station 3800N, SPA400 Sound Proof Housing). The most important step when we captured nanostructure images using SEM is the used coordinates of SEM characterizations must be the same as the before exposed coordinates. Therefore, before we exposed the resist, all exposure parameters are recorded. All of SEM images were captured in as the following parameters: accelerating voltage 20 kV, magnification 30.000X and spot size 52.

3. Results and discussions

In this experiment, mask 4 that were used for point contact formation was spun with positive tone resist of 495 PMMA A4 and the others were spun with negative tone e-beam resist of ma-N 2403.



(a) (b) (c)

Fig. 1: (a) Schematic of mask 1 for doping insulating, (b) SEM image of mask for doping insulating and (c) AFM image of mask for doping insulating.

Figure 1(a) is a schematic drawing of mask 1 for doping insulating. We can compare dimensions of mask 1 in Fig. 1(a) with those of SEM image in Fig. 1(b). Figure 1(b) shows that the lower part width of resist mask 1 is 176 nm and the upper part width of resist mask 1 is 462 nm. In the SEM image, the total length of mask 1 is 798 nm in which the dark part length is 607 nm. The peak height of resist mask 1 is 23.36 nm and the profile line analysis of AFM image of Fig. 1(c) seems uniformly flat. SEM image shows the edges of mask are not sharp and the dimensions are biased of the schematic drawing ones. Insulator mask is used to insulate between phosphorus (P) doped and un-doped area. Many researchers have used implantation mask in their doping processes [9,16]. Kobayashi et. al. (2006) used this SiO_2 mask as suspended mask.

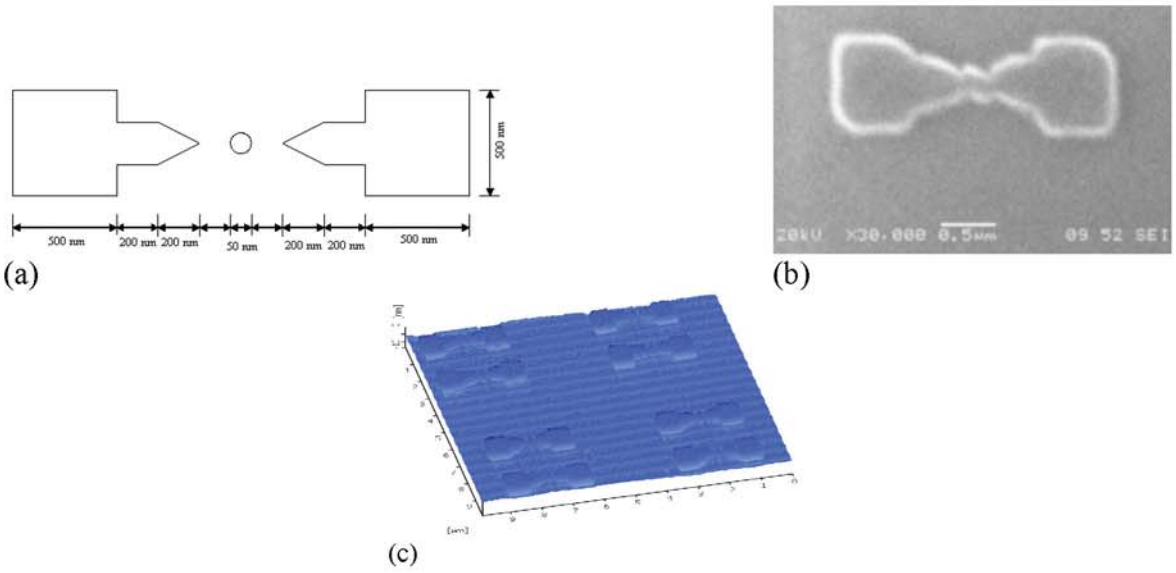


Fig. 2: (a) Schematic of mask 2 for source-QD-drain formation, (b) SEM image of mask of source-QD-drain formation and (c) AFM image of mask of source-QD-drain formation.

Figure 2(a) is a schematic drawing of mask 2 for source-QD-drain formation. Figure 2(b) shows a resist dot between masks of source and drain where the minimum source dimension is 767 nm x 591 nm and the drain dimension is 740 nm x 552 nm. Meanwhile, especially dot diameter in Fig. 2(b) is 297 nm and the dots diameters of AFM images are in the range of 134 nm–161 nm. In three dimensions, these resist nano dots seem cones as shown in Fig. 2(c). We have fabricated many samples and found that the peak height of cone nano dots is in the range of about 10 nm–200 nm. Both of area spaces between source-dot and dot-drain resist mask function as nano constrictions (tunnel barriers). The designs of these spaces were varied to observe the optimum fabrication.

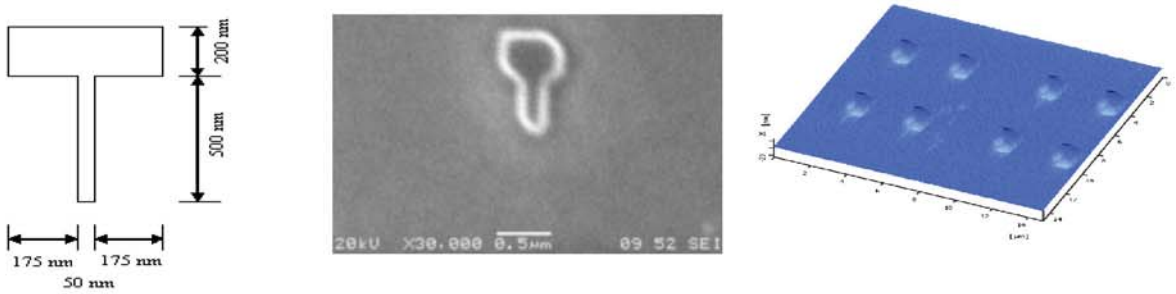


Fig. 3: (a) Schematic of mask 3 for Poly-Si gate formation, (b) SEM image of mask for poly Si gate formation and (c) AFM image of mask for poly Si gate formation.

Figure 3(a) is a schematic drawing of mask 3 for poly-Si top gate formation. Meanwhile, Fig. 2(b) is that of SEM image and Fig. 3(c) is that of AFM image. Design of mask 3 is the same as mask 1 in which this equity is aimed to accurately align. Image in Fig. 3(b) seems narrower than that of Fig. 1(b), in addition, mask 1 is resulted at condition under development and inversely mask 3 is resulted at condition over one. The very low area step size and e-beam dose can result deflected lines of SEM image.

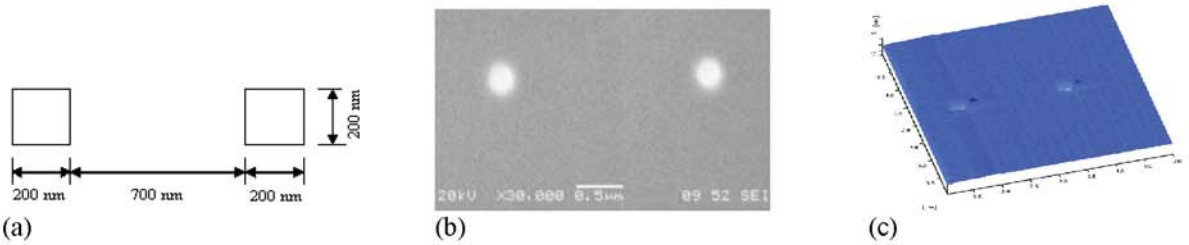


Fig. 4: (a) Schematic of mask 4 for point contact formation, (b) mask for point contact formation and (c) Mask for point contact formation.

Figure 4(a) is a schematic of mask 4 for point contact formation. Figure 4(b) is SEM image of resist mask for point contact formation and Fig. 4(c) is another image by AFM. SEM image of mask 4 shows lighter pattern than background and on the other hand, SEM images of the others show inversely darker pattern than background. In addition, point contact patterns are holes which are spun of positive resist and the others patterns are peaks which are spun of negative resist. The lighter color of pattern lines of negative resist is a trend side profile. The width of negative resist pattern lines can be optimized by focusing SEM. Fig. 4(b) shows the width of point contact mask is 294 nm and the whole depth of mask 4 is 7.41 nm. Schematic of mask 4 are squares but in SEM image seems as circles.

Therewith, we found shape bias of mask schematics and SEM images of mask where according to Hudek & Beyer (2006), this is caused by proximity effect. Therefore, existing correction techniques rely on (i) shot-by-shot modulation of the exposure dose, (ii) modification of pattern geometry (shape bias), or on (iii) combining of both methods [8].

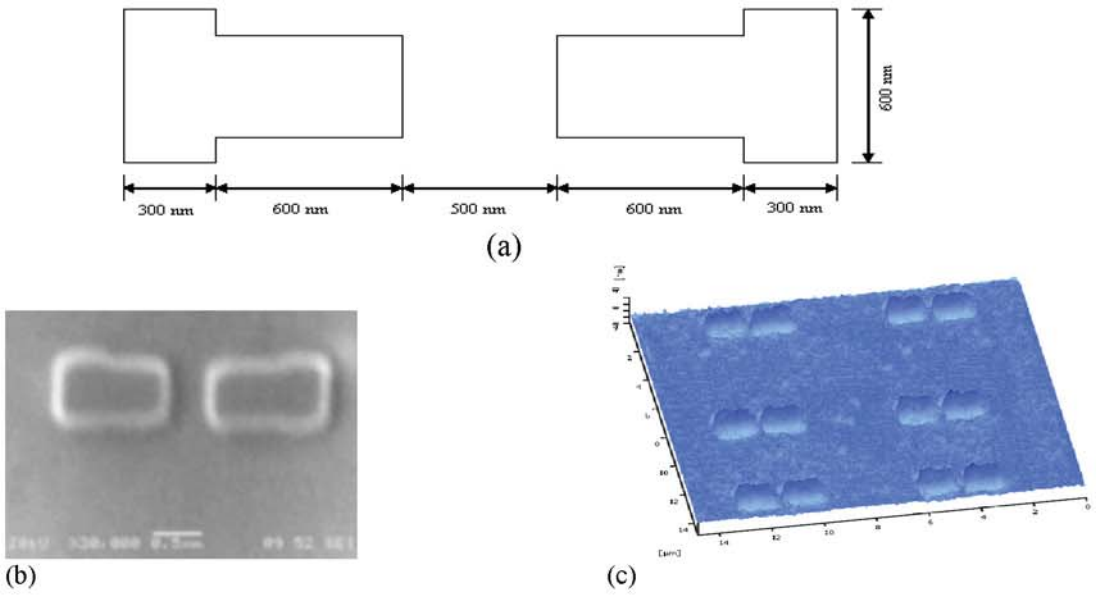


Fig. 5: (a) Schematic of mask 5 for Al metal pad formation, (b) mask for Al metal pad formation and (c) mask for Al metal pad formation.

Metal pad mask of this SET design is schematically drawn as shown in Fig. 5(a). Figure 5(b) where both shows the AFM image of mask for metal pad formation, and aluminium is the alternative metal pad material. The dimensions of this mask are as the followings: side width of 693 nm, center width of 568 nm and the length of 1.206 nm. In three di-

mensions, Fig. 5(c) shows the peak height of resist mask of 14.41 nm. Equipment-related parameters are also critical in nano-patterning, when a variable-shape pattern generator is used for resist exposure. All of masks show that the line edges are not sharp. In this context, the line edges were defined by the shape of the circle beam shots. Therefore, to improve edge line sharpness, it is recommended to use a rectangular beam shots. The line-edge roughness is defined mainly by the shape of the rectangular beam shots, and the stitching errors at the joint-point of two shots. These two problems are influenced by the quality of the rectangular apertures and the alignment of the e-beam formation system [14].

4. Conclusions

Direct write e-beam lithography is a useful technique for fabrication of QD SET masks with small critical dimension. The EBL resolution is limited not by e-beam diameter, but by a combination of proximity effects, resist chemistry, and the e-beam alignment. In this work, the direct e-beam lithography process was optimized to fabricate different types of masks. The fabrication of both cone nano dots in the range of 134 nm–161 nm for negative resist and fabrication of point contacts of 294 nm for positive resist has also been demonstrated. The others masks have been fabricated of negative resist in the range above 153 nm.

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References

[1] S. Altmeyer, B. Spangenberg, F. Kühnel, H. Kurz, Microelectron. Eng. **30** (1996) 399
[2] T. Berrer, D. Pachinger, G. Pillwein, M. Mühlberger, H. Lichtenberger, G. Brunthaler, F. Schäffler, Physica E **34** (2006) 456
[3] M. Dilger, R.J. Haug, K.V. Klitzing, Semicond. Sci. Technol. **11** (1996) 1493
[4] Z. A. K. Durrani, Physica E **17** (2003) 572
[5] E. G. Emiroglu, D. G. Hasko, D. A. Williams, Microelectron. Eng. **73-74** (2004) 701
[6] Y. Furuta, H. Mizuta, T. Kamiya, Y. T. Tan, K. Nakazato, Z. A. K. Durrani, K. Taniguchi, ESSDERC (2002) 399
[7] U. Hashim, Sutikno, & Z. A. Z. Jamal, Proc. of ICMNS'06 ITB (2006)
[8] P. Hudek, D. Beyer, Microelectron. Eng. **83** (2006) 780
[9] F. E. Hudson, A. J. Ferguson, D. N. Jamieson, A. S. Dzurak, R. G. Clark, Microelectron. Eng. **83** (2006) 1809
[10] S. F. Hu, G. J. Wang, Y. P. Fang, Z. Y. Pan, Y. C. Chou, Chinese J. Phys. **42** (2004) 636
[11] Y. Ito, H. Tsuyoshi, N. Anri, Yokoyama, Appl. Phys. Lett. **80** (2002) 4617
[12] S. Kobayashi, M. Imaeda, S. Matsumoto, Mater. Sci. Eng. C **26** (2006) 889
[13] A. Kowalik, Z. Jaroszewcz, A. Kolodzejcyk, Microelectron. Eng. **77** (2005) 347

[14] I. Kostic, R. Andok, V. Barak, I. Caplovic, A. Konecnikova, L. Matay, P. Hrkut, A. Ritomsky, J. Mater. Sci. **14** (2003) 645
[15] K. Kurihara, H. Namatsu, M. Nagase, T. Makino, Microelectron. Eng. **35** (1997) 261
[16] M. Mitic., S. E. Andresen, C. Yang, T. Hopf, V. Chan, E. Gauja, F. E. Hudson, T. M. Buehler, A. J. Ferguson, C. I. Pakes, S. M. Hearne, G. Tamanyan, D. J. Reilly, A. R. Hamilton, D. N. Jamielson, A. S. Dzurak, R. G. Clark, Microelectron. Eng. **78-79** (2005) 279
[17] A. Notargiacomo, L. D. Gaspare, G. Scappucci, G. Mariottini, E. Giovine, F. Evangelisti, Mater. Sci. Eng. C **23** (2003) 671
[18] L. Palun, S. Tedesco, M. Heitzman, F. Martin, D. Fraboulet, B. Dal'zotto, M. E. Nier, P. Mur, T. Charvolin, Microelectron. Eng. **53** (2000) 167
[19] T. R. Stevenson, W. T. Hsieh, M. J. Li, K. W. Rhee, R. J. Schoelkopf, C. M. Stahle, J. D. Teufel IEEE Trans. Appl. Supercond. **13** (2003) 1139
[20] Y. Takahashi, Y. Ono, A. Fujiwara, H. Inokawa, NTT Technical Review **2** (2004) 21
[21] M. G. Tanner, E. G. Emiroglu, D. G. Hasko, D. A. Williams, Microelectron. Eng, **78-79** (2005) 195
[22] T. Weinmann, H. Scherer, P. Hinze, J. Niemeyer, Microelectron. Eng. **53** (2000) 225
[23] L. Zhuang, L. Guo, S. Y. Chou, Appl. Phys. Lett. **72** (1998)1205